8,388,608 WORD X 36 BIT (EDO) DYNAMIC RAM MODULE

Description

The THM3680G5BS/BSG is a 8,388,608 words by 36 bits dynamic RAM module which assembled 16 pcs of TC5117405BSJ and 2 pcs of TC5117445BSJ on the printed circuit board. This module is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and as image memory systems, and to the others which are requested compact size.

Features

- 8,388,608 word by 36 bit organization
- Fast access time and cycle time
- Single power supply of 5V±5%
- Low Power
  - 4,620mW MAX. Operating
  - (THMxxxxxx-60)
  - 3,990mW MAX. Operating
  - (THMxxxxxx-70)
  - 42mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh and Hyper Page Mode (EDO) and Test Mode capability
- All inputs and outputs TTL compatible
- 2,048 refresh cycles/32ms
- Package
  - THM324005BS - xx: 2nd Gen. 72pin SIMM (Tin-Lead Contact)
  - THM324005BSG - xx: 2nd Gen. 72pin SIMM (Gold Contact)

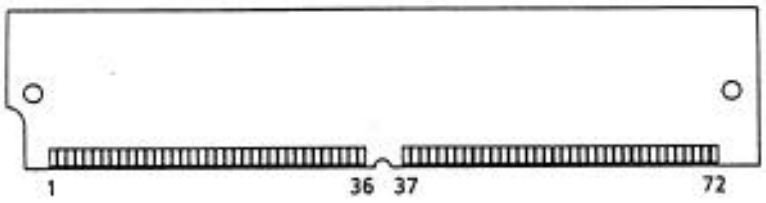
Key Parameters

Item		THM3680G5BS/BSG	
		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{AA}	Column Address Access Time	30ns	35ns
t_{CAC}	$\overline{CAS}$ Access Time	17ns	20ns
t_{RC}	Cycle Time	104ns	124ns
t_{HPC}	Hyper Page Mode Cycle Time	25ns	30ns

Pin Name

A0~A10	Address
DQ0~DQ35	Data Input/Output
$\overline{CAS0}$~$\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$, $\overline{RAS1}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
PD	Presence Detect Pin
NC	No Connection

Pin Connection



1	V_{SS}	10	V_{CC}	19	A10	28	A7	37	DQ17	46	NC	55	DQ12	64	DQ34
2	DQ0	11	NC	20	DQ4	29	NC	38	DQ35	47	$\overline{W}$	56	DQ30	65	DQ16
3	DQ18	12	A0	21	DQ22	30	V_{CC}	39	V_{SS}	48	NC	57	DQ13	66	NC
4	DQ1	13	A1	22	DQ5	31	A8	40	$\overline{CAS0}$	49	DQ9	58	DQ31	67	PD0
5	DQ19	14	A2	23	DQ23	32	A9	41	$\overline{CAS2}$	50	DQ27	59	V_{CC}	68	PD1
6	DQ2	15	A3	24	DQ6	33	NC	42	$\overline{CAS3}$	51	DQ10	60	DQ32	69	PD2
7	DQ20	16	A4	25	DQ24	34	NC	43	$\overline{CAS1}$	52	DQ28	61	DQ14	70	PD3
8	DQ3	17	A5	26	DQ7	35	DQ26	44	$\overline{RAS0}$	53	DQ11	62	DQ33	71	NC
9	DQ21	18	A6	27	DQ25	36	DQ8	45	$\overline{RAS1}$	54	DQ29	63	DQ15	72	V_{SS}

	-60	-70
PD0	NC	NC
PD1	V_{SS}	V_{SS}
PD2	NC	V_{SS}
PD3	NC	NC

Electrical Characteristics and Recommended AC Operating Conditions (V_{CC} = 5V ± 10%, Ta = 0 ~ 70°C) (Notes 6,7,8)

SYMBOL	PARAMETER	TC5118165BJ/BFT				UNIT	NOTES
		-60		-70			
		MIN	MAX.	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	104	-	124	-	ns	
t_{RMW}	Read-Modify-Write Cycle	135	-	157	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	60	-	70	ns	9,14,15
t_{CAC}	Access Time from $\overline{CAS}$	-	17	-	20	ns	9,14
t_{AA}	Access Time from Column Address	-	30	-	35	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	35	-	40	-	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	15	ns	10
t_T	Transition Time (Rise and Fall)	1	50	1	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	40	-	50	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	100,000	70	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	10	-	12	-	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge (Fast Page Mode)	35	-	40	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	40	-	50	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	10	10,000	12	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	14	43	14	50	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	12	30	12	35	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5		ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	15	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	-	35	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	ns	11
t_{WCH}	Write Command Hold Time	10	-	12	-	ns	

Electrical Characteristics and Recommended AC Operating Conditions (Cont)

SYMBOL	PARAMETER	TC5118165BJ/BFT				UNIT	NOTES
		-60		-70			
		MIN	MAX.	MIN	MAX		
t_{WP}	Write Command Pulse Width	10	-	12	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	12	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	12	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	ns	12
t_{DH}	Data Hold Time	10	-	12	-	ns	12
t_{REF}	Refresh Period	-	16	-	16	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	36	-	39	-	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	79	-	89	-	ns	13
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	49	-	54	-	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	54	-	59	-	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	15	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	-	5	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle	20	-	20	-	ns	
t_{ROH}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	10	-	10	-	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	15	-	20	ns	9
t_{OED}	$\overline{OE}$ to Data Delay	15	-	15	-	ns	
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	0	-	0	-	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	15	0	15	ns	10
t_{OEH}	$\overline{OE}$ Command Hold Time	10	-	12	-	ns	
t_{ODS}	Output Disable Set-Up Time	0	-	0	-	ns	

Electrical Characteristics and Recommended AC Operating Conditions

SYMBOL	PARAMETER	TC5118165BJ/BFT				UNIT	NOTES
		-60		-70			
		MIN	MAX.	MIN	MAX		
t_{RNCD}	$\overline{RAS}$ to next $\overline{CAS}$ Delay Time (Hyper Page Mode)	60	-	70	-	ns	
t_{HPC}	Hyper Page Mode Cycle Time	25	-	30	-	ns	
t_{HPRWC}	Hyper Page Mode Read-Modify-Write Cycle Time	68	-	75	-	ns	
t_{COH}	Output Data Hold Time	5	-	5	-	ns	
t_{REZ}	Output Buffer Turn-off Delay from $\overline{RAS}$	0	15	0	15	ns	10, 16
t_{WEZ}	Output Buffer Turn-off Delay from $\overline{WE}$	0	15	0	15	ns	10
t_{WED}	$\overline{WE}$ to Data Delay	15	-	15	-	ns	
t_{OE}	$\overline{OE}$ Pulse Width	15	-	20	-	ns	
t_{OEP}	$\overline{OE}$ Precharge Time	10	-	12	-	ns	
t_{CPO}	$\overline{RAS}$ to $\overline{OE}$ Precharge	5	-	5	-	ns	

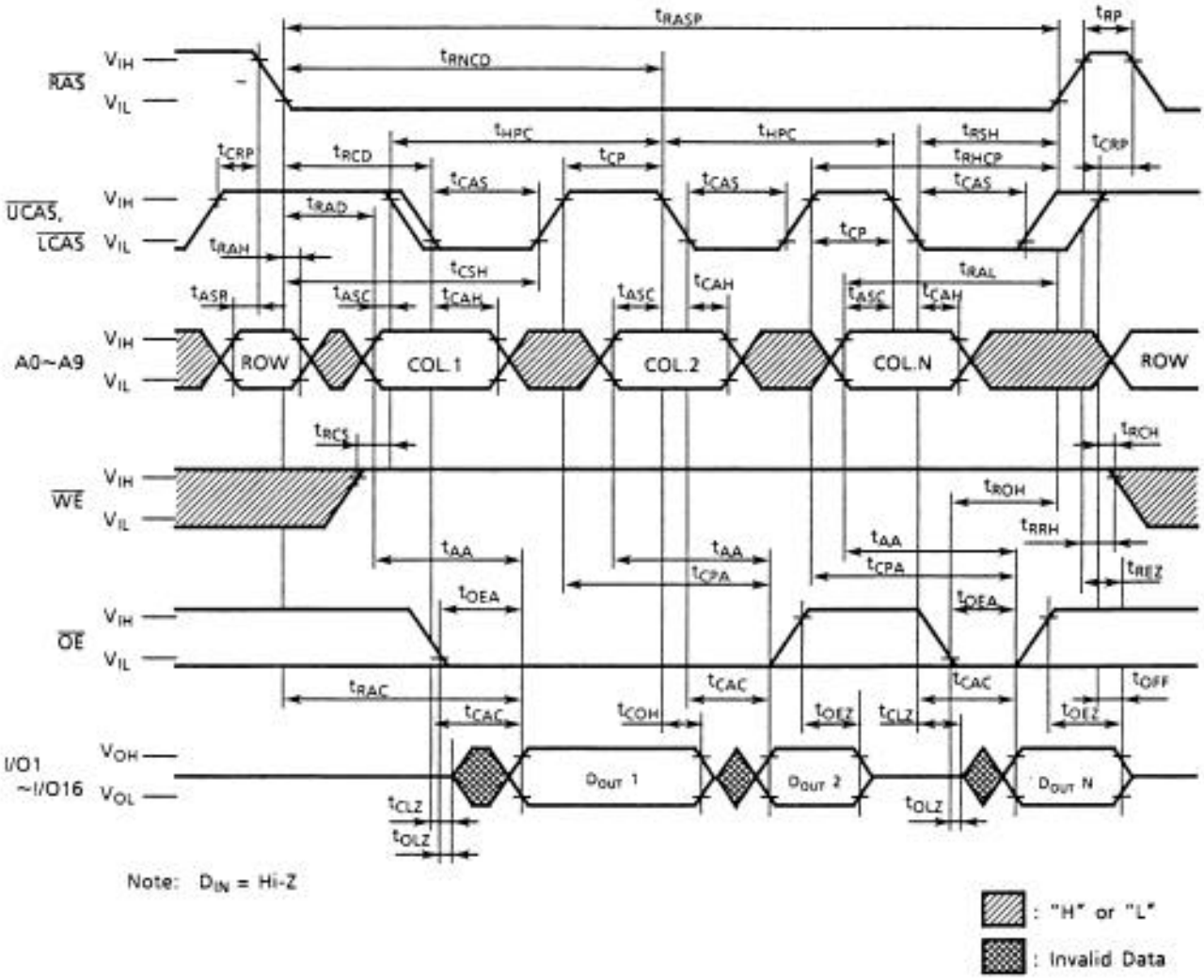
Capacitance (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{I1}	Input Capacitance (A0 ~ A9)	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{WE}$, $\overline{OE}$)	-	7	
C_O	Input Capacitance (I/O1 ~ I/O16)	-	7	

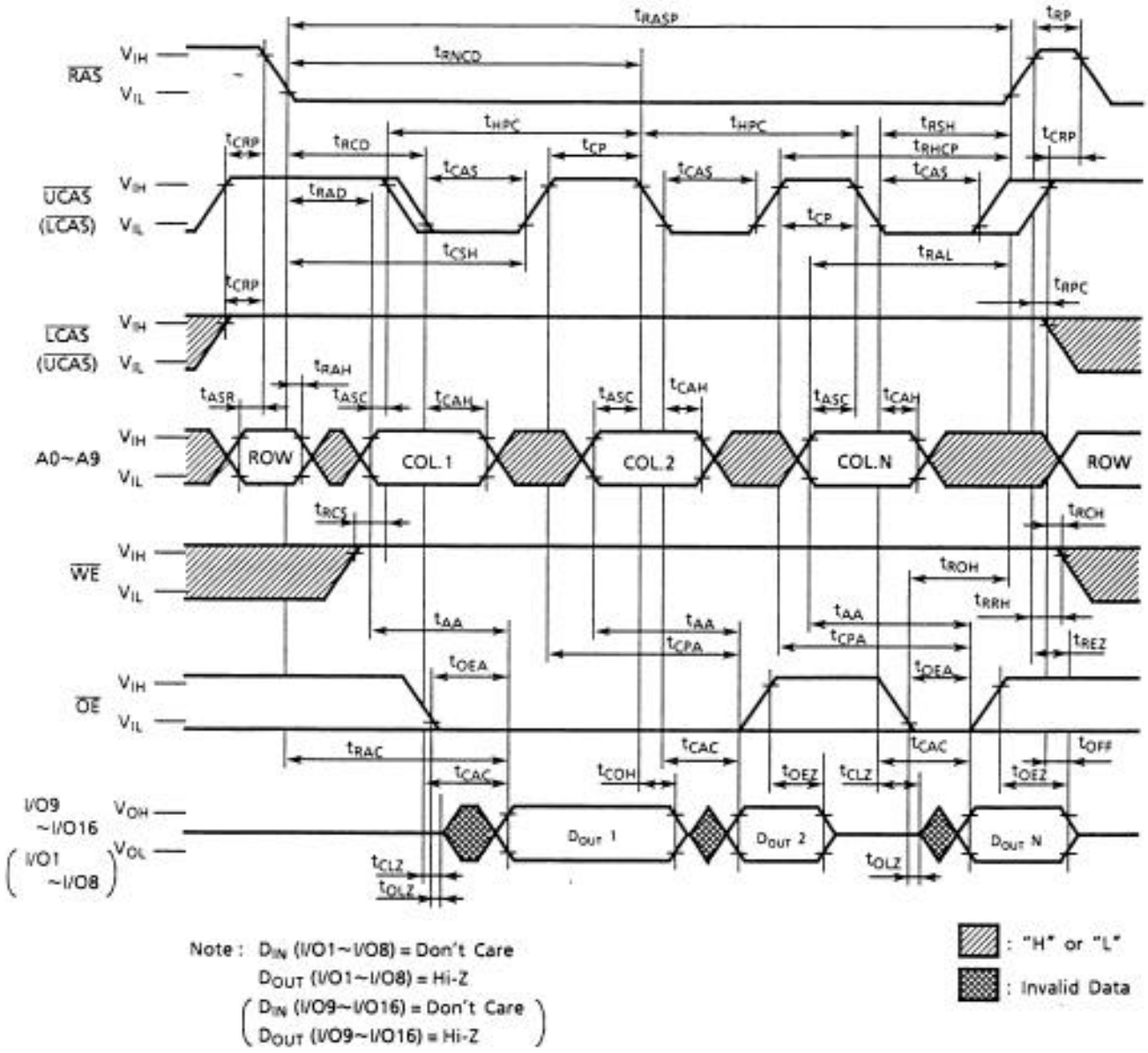
Notes:

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Address can be changed one or less while $\overline{RAS}=V_{IL}$. In case of I_{CC4}, it can be changed once or less during a hyper page mode cycle (t_{PC}).
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.
7. AC measurements assume t_T=2ns.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{UCAS}$, $\overline{ULAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in Read-Modify-Write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data output will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.), $t_{AWD} \geq t_{AWD}$ (min.) and $t_{CPWP} \geq t_{CPWD}$ (min.), (Hyper Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of condition is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.
16. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going (t_{OFF}). If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going (t_{REZ}).

Hyper Page Mode Read Cycle

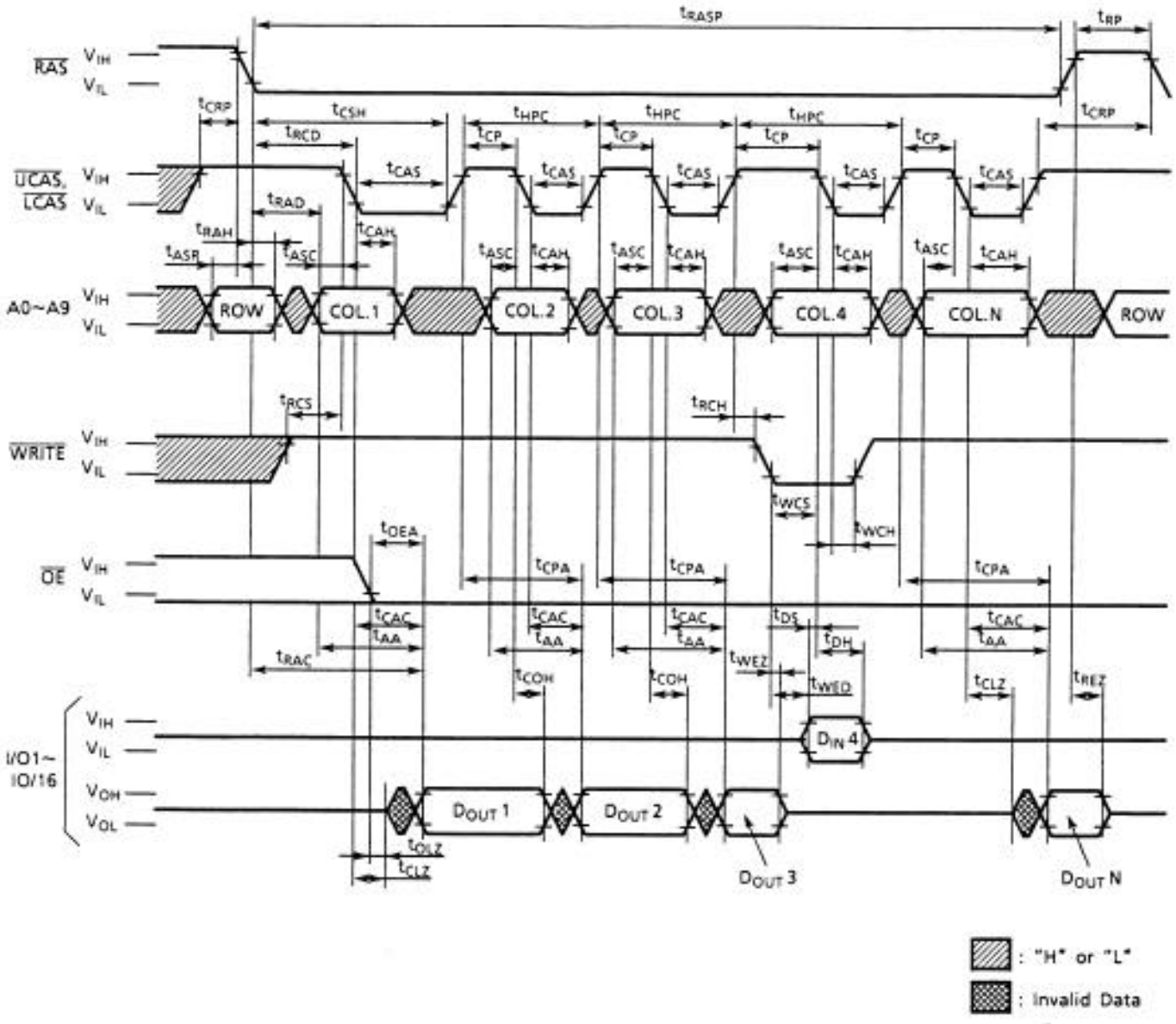


Hyper Page Mode Byte Read Cycle

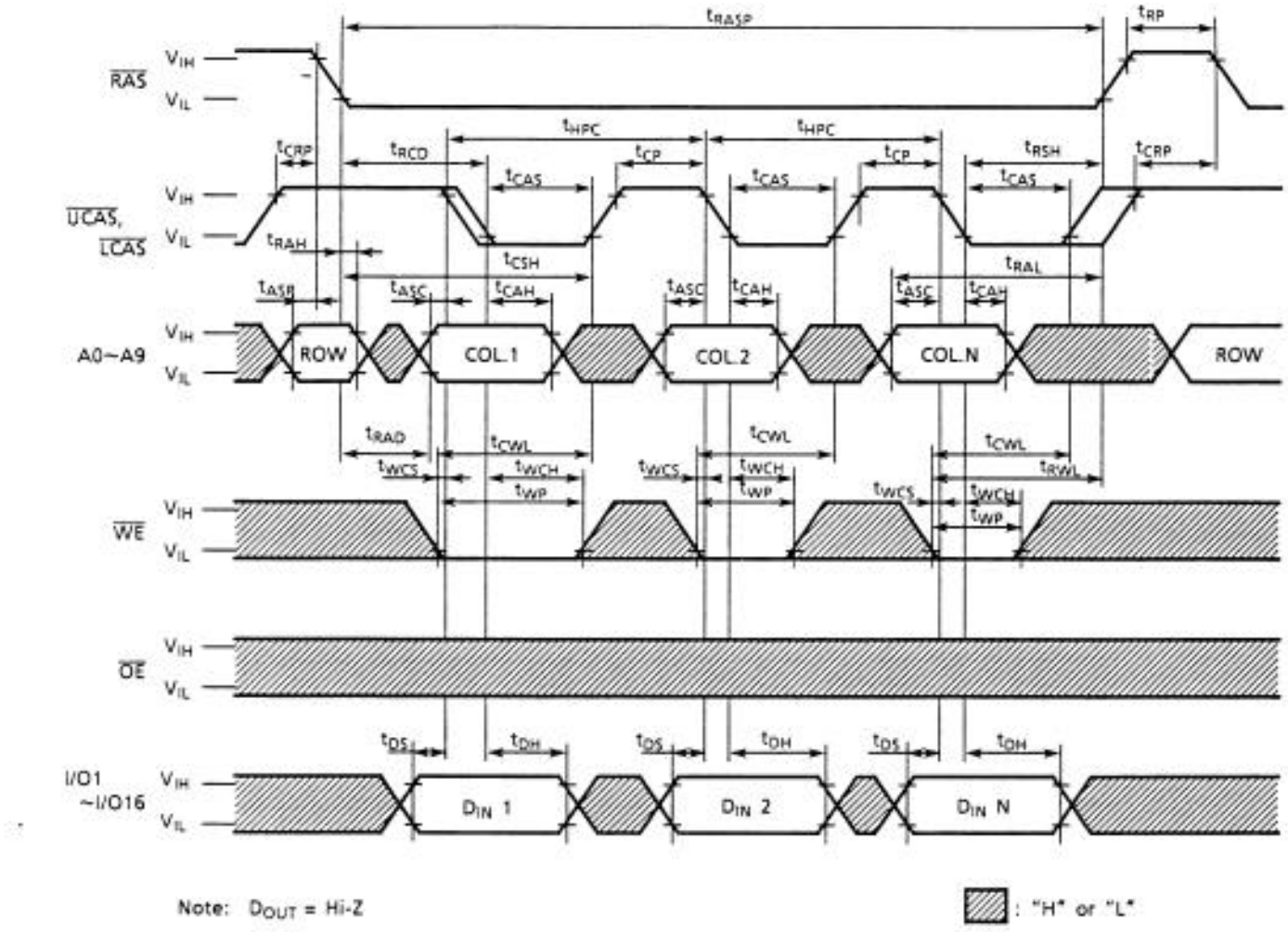


Note : D_{IN} (I/O1~I/O8) = Don't Care
D_{OUT} (I/O1~I/O8) = Hi-Z
(D_{IN} (I/O9~I/O16) = Don't Care
D_{OUT} (I/O9~I/O16) = Hi-Z)

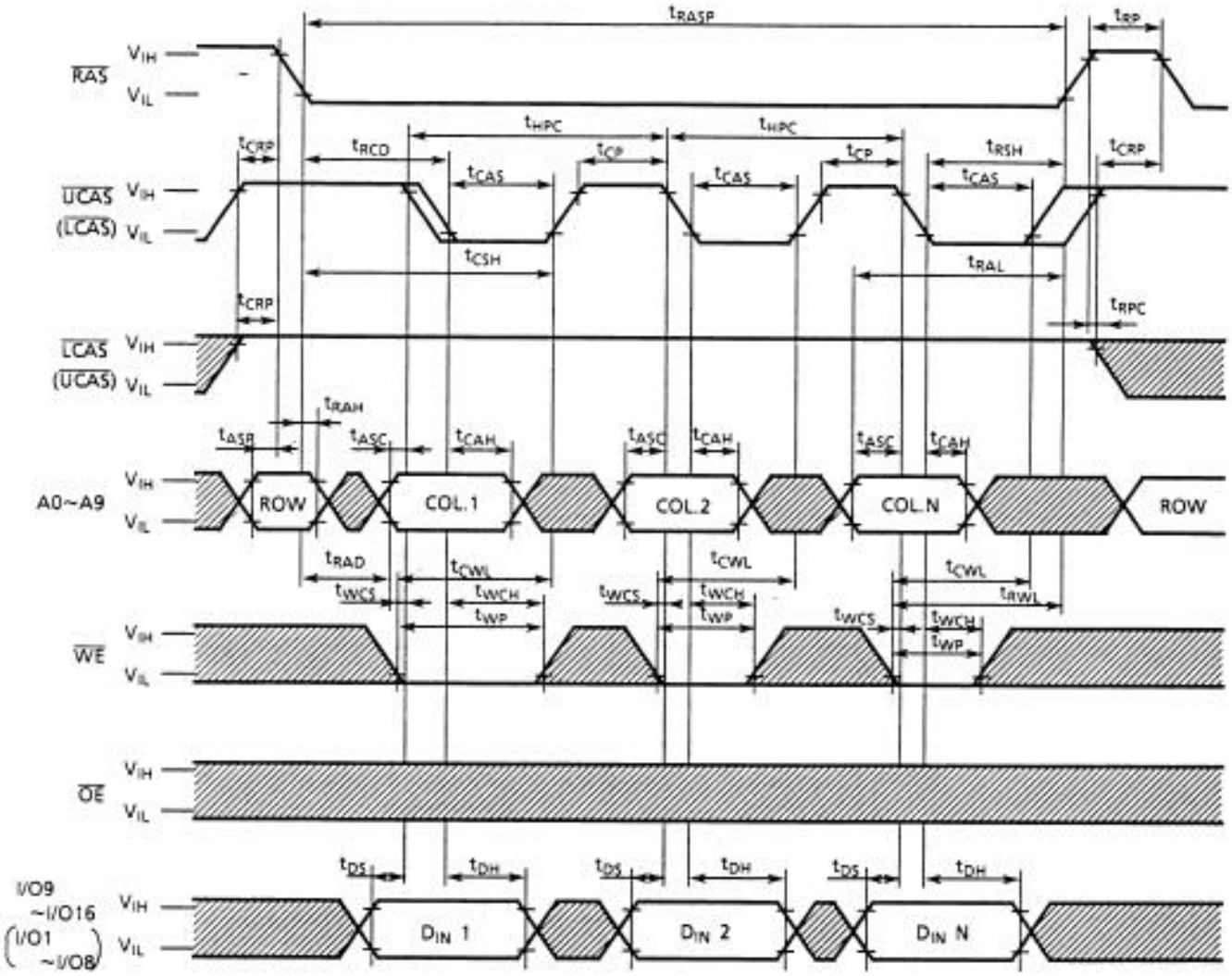
Hyper Page Mode Read Write Mixed Cycle



Hyper Page Mode Write Cycle (Early Write)



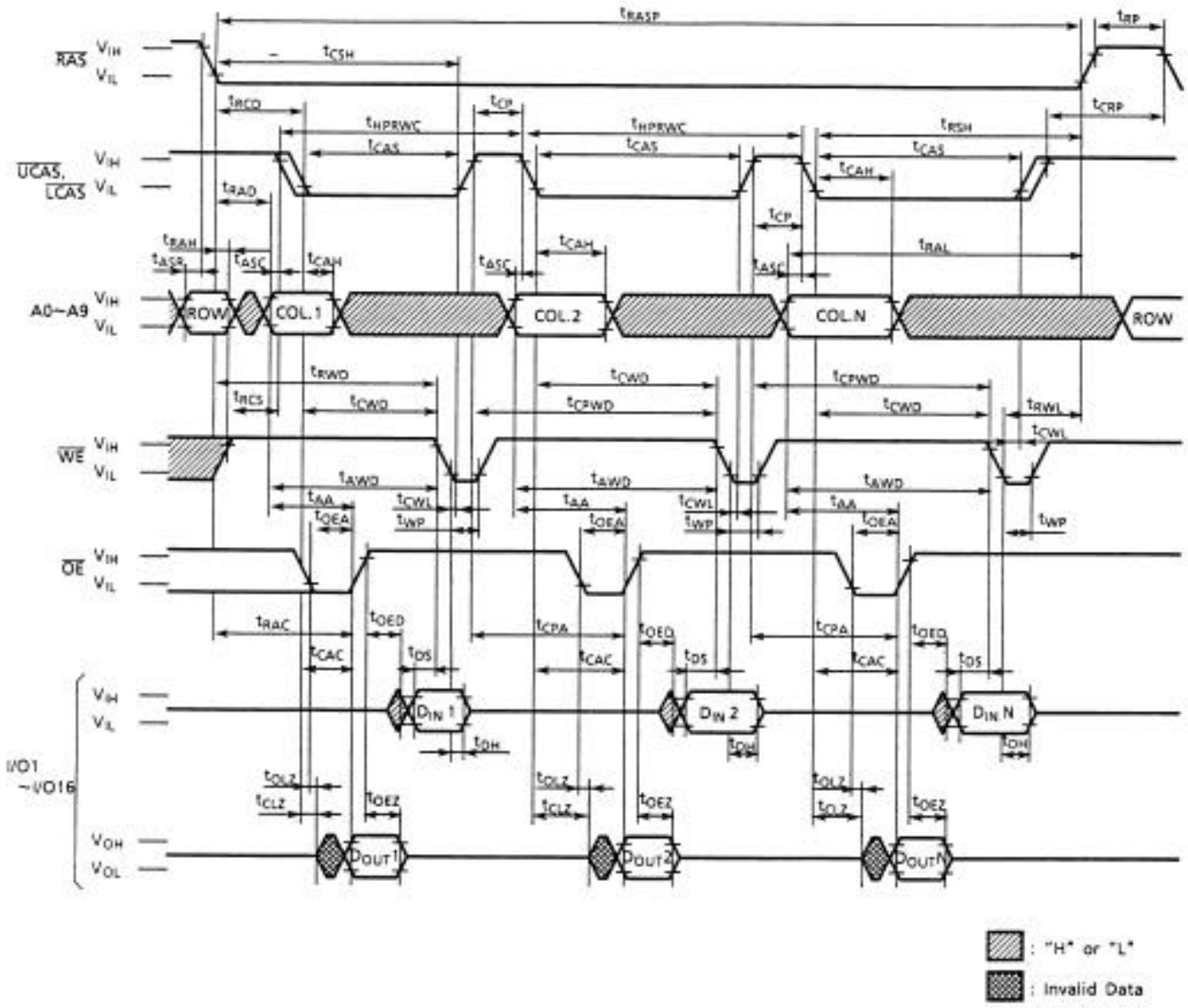
Hyper Page Mode Byte Write Cycle (Early Write)



Note : D_{IN} (I/O1~I/O8) = Don't Care
(D_{IN} (I/O9~I/O16) = Don't Care)
D_{OUT} = Hi-Z

: "H" or "L"

Hyper Page Mode Read-Modify-Write Cycle



Hyper Page Mode Byte Read-Modify-Write Cycle